Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	2	extending near5 clock adj (pulse or cycle) with wait	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 10:38
L15	114	"waiting state" and microcontroller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 10:52
L16	44	L15 and ("read only memory" or ROM)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 10:54
L17	10451	wait adj state	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 10:55
L18	777	(wait adj state) with clock	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 10:55
L19	120	18 and microcontroller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 11:02
L20	0	18 and (extend$3 near5 (clock adj pulse))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 11:01
L21	296	(extend$3 near5 (clock adj pulse))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 11:01

L22	5	21 and microcontroller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 12:37
L23	8	21 and (external adj memory)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 11:05
L24	31	(clock adj state) near5 remain$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 12:36
L25	143	insert$3 near5 wait near5 clock	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 12:45
L26	19	25 and microcontroller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 12:42
L27	0	(wait adj state) with extending with (clock adj pulse)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 12:44
L28	208	extending with (clock adj pulse)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 12:44
L29	0	28 and ("wait state")	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 12:45

L30	0	28 and (wait adj state)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/03 12:45
S1	2	"20040225851"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 15:25
S2	2	chang-sheng-tsai.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 15:26
S3	5	chi-chao-wen.in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 15:27
S4	9180	"waiting state"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:35
S5	114	"waiting state" and microcontroller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 15:29
S6	44	S5 and ("read only memory" or ROM)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:43
S7	7	S6 and (external near5 (memory or storage))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 08:28

S8	3799	micro$1controller.ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:06
S9	26	S8 and (wait$3 near2 state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:32
S10	6167	cycle near2 extend$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:33
S11	6	S8 and S10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:08
S12	19219	wait$3 adj state	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:36
S13	212	S10 and S12	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:36
S14	0	S8 and S13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:36
S15	17	S13 and micro$1controller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:42
S16	11	S15 and ("read only memory" or ROM)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:43

S17	8	S16 and (external near5 (memory or storage))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/28 16:43
S18	114	"waiting state" and microcontroller	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 07:39
S19	44	S18 and ("read only memory" or ROM)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 07:39
S20	676	insert$3 with (wait$3 adj state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 09:30
S21	339	S20 and ("read only memory" or ROM)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 09:00
S22	116	S21 and ("external memory")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 09:01
S23	71	S22 and (address$3 near2 range$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 09:02
S24	26	S23 and micro$1controller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 09:29
S25	3799	micro$1controller.ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 09:29

S26	676	S20 with ((wait$3 adj state) or (extend$3 near2 clock) or (cycle steel))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 09:31
S27	131	S26 and (("read only memory" or rom) and (external near2 memory))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 10:01
S28	2326	(check$3 or determ$3) with range with address	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 09:34
S29	7	S27 and S28	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 09:34
S30	105	S27 and (micro$1controller or micro$1computer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/29 10:02
S31	4547	(determin$3 or judg$3 or check$3) with address with range	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 16:51
S32	281	S31 and "wait state"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 16:46
S35	52	S32 and ("serial interface")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 16:47
S36	16	S35 and micro$1controller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 16:48
S37	0	S31 and "wait$3 state"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 16:47

S38	291	S31 and wait$3 adj state	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 16:47
S39	53	S38 and ("serial interface")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 16:47
S40	31	S39 and ((memory near2 controller) or MMU)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 16:48
S41	15	S40 and (micro$1controller or (micro$1computer))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/29 16:49
S42	15	S41 and (determin$3 or judg$3 or check$3) with address with range	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 06:27
S43	4547	(determin$3 or judg$3 or check$3) with address with range	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 06:28
S44	20929	(wait$3 adj state)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 06:29
S45	291	S43 and S44	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 06:29
S46	498138	micro$1controller or micro$1processor or micr$1computer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:04
S47	191	S45 and S46	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 06:31

S48	140	S47 and ("read only memory" or ROM)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 06:32
S49	59	S48 and (memory near2 interface)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 06:32
S50	219966	(micro$1controller or micr$1computer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:05
S51	27049	(micro$1controller or micr$1computer).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:05
S52	94405	(micro$1controller or micr$1computer).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:26
S53	81	S43 and S52	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:05
S54	7	S44 and S53	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:26
S55	7	S45 and S52	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:26
S56	1629	(micro$1controller or micr$1computer) with (on$1chip or internal adj ("read only memory" or ROM))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:28
S57	1	S45 AND S56	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:31

S58	309	EXTEND$3 WITH (ADDRESS NEAR2 RANGE)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:32
S59	16	S56 AND S58	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:32
S60	10	S59 and "wait state"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 07:32
S61	5	"checking range" near5 address	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 08:29
S62	565	check$3 near5 range near5 address	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 08:31
S63	6	S56 and S62	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 08:30
S64	2173	(check$3 or determin$3) near5 range near5 address	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 11:07
S65	12	S56 and S64	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 08:34
S66	0	extending with (micro$1controller or micro$1computer) with (clock adj cycle)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 08:36

S67	130	extending with (clock adj cycle)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 08:38
S68	0	S56 and S67	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 08:36
S69	3799	micro$1controller.ti.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 08:39
S70	24	S44 and S69	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 08:46
S71	2	S45 and (ready near2 flag)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/07/30 08:47
S72	127300	range near5 signal	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 09:20
S73	123	range near5 checking near5 signal	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 09:21
S74	2	S44 and S73	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 09:21
S75	241	extend$3 near5 (clock adj cycle)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:22

S76	30	S50 and S75	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:14
S77	2	S51 and S75	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:14
S78	27	extending near5 (clock adj cycle)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:43
S79	7	"clock steel"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:33
S80	3	S51 and (extending near5 clock)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:30
S81	110	"cycle steel"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:34
S82	0	S51 and S81	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:34
S83	0	S52 and S81	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:34
S84	25706	711/1-3,101-105,111-115,,167.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:50
S85	909	S43 and S84	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:50

S86	90	S44 and S85	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:53
S87	771	712/1,38,43.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:56
S88	6	S45 and S87	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 10:56
S89	2	"20030221062"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/07/30 11:33
S90	393	(check$3 or determin$3) near5 (range near5 address) near5 (circuit$3 or logic or unit)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 11:08
S92	503439	micro$1controller or micro$1computer or micro$1processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 11:11
S93	205	S90 and S92	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/02 11:10
S94	28672	wait$3 near2 state	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 11:11
S95	37	S93 and S94	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 14:05

S96	1227	range near2 checking	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 13:10
S97	100	address near5 range near2 checking	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 13:21
S98	794	ready adj flag	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 13:11
S99	1	S97 and S98	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 13:11
S100	2	address with (range near2 checking near2 signal)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 13:23
S101	2	address with (range near2 checking near2 (signal or indicator or flag))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 13:24
S102	17	address with (range near5 checking near5 (signal or indicator or flag))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/08/02 13:24
S103	17	S95 and comparator	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/08/02 14:05